AMENDMENTS TO THE DRAWINGS

The drawings are objected to as failing to comply with 37 CFR 1.121(d) because the word "Global" is misspelled in "Globle Bit Line" of FIG. 1A. A replacement sheet has been included with this response correcting the misspelling.

REMARKS

Claim Rejections Under 35 U.S.C. § 103

Claims 1-13, 16, 18-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Acharya et al.* (U.S. Patent No. 6,055,184) in view of *Bruce et al.* (U.S. Patent No. 6,529,416). Claims 14, 15 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Acharya et al.* (U.S. Patent No. 6,055,184) in view of *Bruce et al.* (U.S. Patent No. 6,529,416) and in further view of *Mihara* (U.S. Patent No. 6,735,119). Applicants respectfully traverse this rejection.

Claims 1, 6, 11, 13, 19, and 21 have been amended to add the limitation that the erase tags stop an erase pulse from being received from tagged memory blocks. This subject matter is disclosed in the specification at paragraph 0029. Therefore, no new matter has been entered by this amendment.

Acharya et al. disclose a memory device having parallel erase operation capability. At col. 5, lines 7-10 of *Acharya et al.*, they state that the tags are utilized to select a sector for erase. *Acharya et al.*, therefore, neither teaches nor suggests Applicants' invention as claimed in the amended claims.

Applicants' claimed invention provides erase tags that indicate a memory block of a particular memory device has already been erased. Additionally, the present claimed erase tags prevent an erase pulse from reaching a memory block that has been tagged. This is neither taught nor suggested by *Acharya et al.*

Bruce et al. disclose a parallel erase operation in a flash memory system 10. *Bruce et al.*, however, neither teach nor suggest Applicants' invention as claimed in the amended claims. Even if it were obvious to combine *Acharya et al.* with *Bruce et al.*, and Applicants maintain that it is not, the combination still would not anticipate Applicant's invention as claimed in the amended claims since the combination does not disclose erase tags that prevent an erase pulse from reach a memory block to which an erase pulse has been transmitted.

Mihara discloses a nonvolatile semiconductor memory. Even if it were obvious to combine *Mihara* with either *Bruce et al.* and/or *Acharya et al.*, and Applicants maintain that it is not, the combination still would not anticipate Applicants' invention as claimed in the amended claims.

Paragraph 16 of the specification has been amended to correct a typographical error. The clocking circuitry was inadvertently labeled "138" instead of "160". The reference number "138" was already used to define a bit line driver. The replacement sheet for Figure 1A has been included with this response and includes this correction as well as the spelling correction of "GLOBAL BIT LINE" as required by the Examiner. No new matter has been entered by these corrections.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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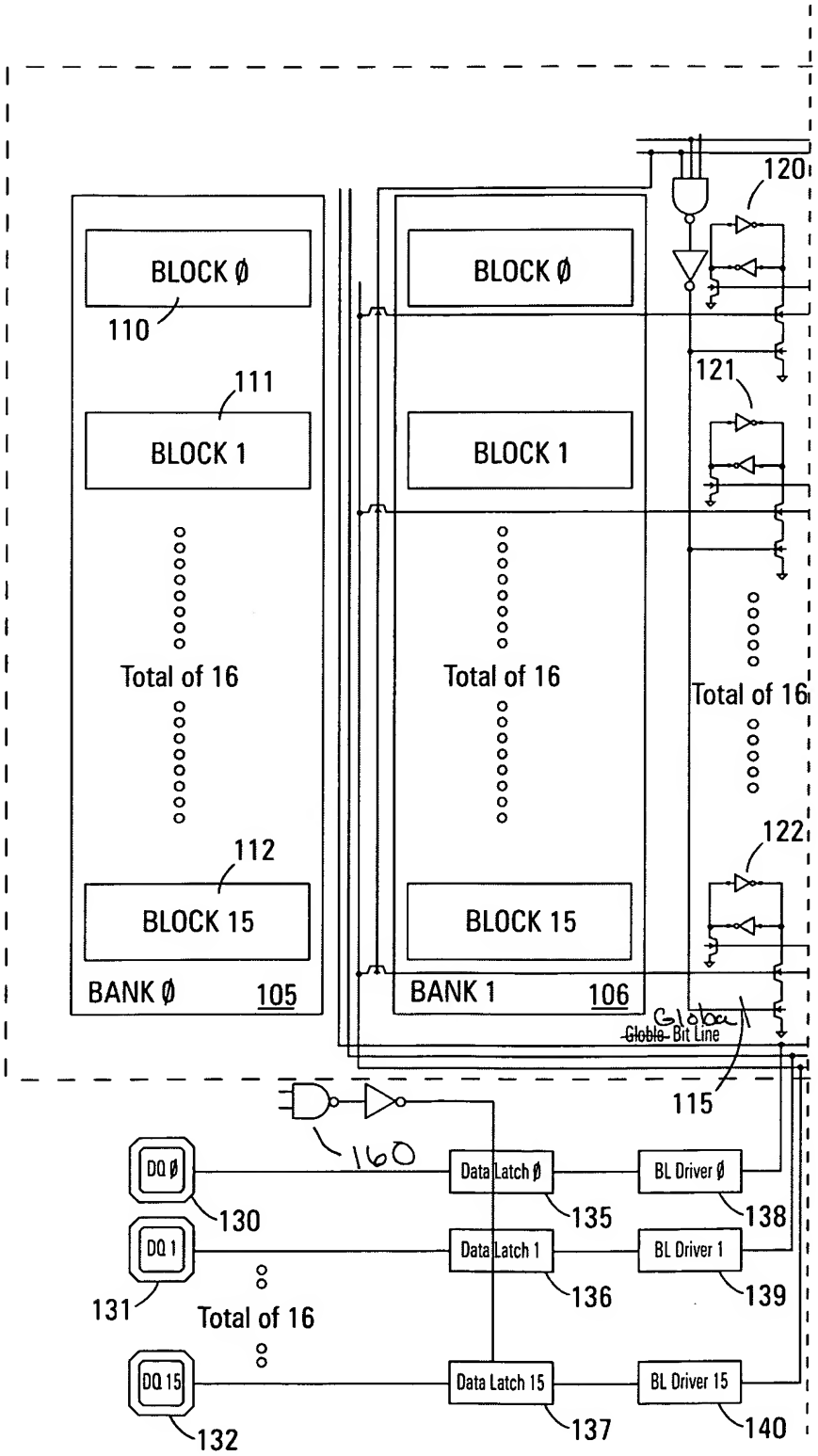

Fig. 1A